

Contents

Introduction	1
Jitter Theory	3
Introduction	3
What Is Jitter?	4
Measuring Jitter	4
The Unit Interval	5
How Can You See Jitter?	6
Jitter in Sampling Processes.	7
Jitter in the Interface: Data Recovery	8
Jitter in Clock Recovery for Synchronization	8
Digital Interface Jitter	8
Intrinsic Jitter	9
Cable-Induced Jitter	10
Data Jitter	11
Preamble Jitter	13
Interfering-Noise-Induced Jitter.	13
Jitter Tolerance	15
The Jitter Transfer Function and Jitter Gain	16
Non-Linear Jitter Behavior	17
Jitter Accumulation.	17
Sampling Jitter	19
Sampling Jitter and the External Clock	19
Time-Domain Model.	20
Frequency-Domain Model	22
Influence of ADC/DAC Architecture	24

Oversampling Converters	24
Noise-Shaping and One-Bit Converters	26
Reducing Jitter Sensitivity in Delta-Sigma Converters.	28
Switched-Capacitor Filters	28
Multi-Bit Noise-Shaped Converters	28
Jitter-Induced Amplitude Modulation	29
Sampling Jitter in Rate Converters	30
Virtual Timing Resolution.	30
Virtual Jitter Attenuation Characteristic	30
Sampling Jitter Transfer Function.	31
Other Points to Note	33
Sampling Jitter / Data Jitter Susceptibility.	33
References	37
Analog-to-Digital Converter Measurements	39
Introduction.	39
Level Measurements in the Digital Domain	39
Digital Full Scale	39
Decibels, Full Scale: dB FS.	40
Using dB FS When Full Scale Is Unattainable	41
Digital Peak Level Metering	
Using Sample Values	41
RMS Metering	43
Quasi-Peak Signal Level Metering	44
Measurement Techniques	44
Notes on the APWIN Procedure Examples	44
Gain	45
Noise	53
High-Level Non-Linear Behavior	63
Low-Level Non-Linear Behavior	68
Jitter Modulation	71
The Fourier Transform	75
Windowing.	78
Signal Frequency Post-Acquisition Scaling	81
Interpretation of Noise in FFT Power Spectra	81
Power Averaging	83
Synchronous Averaging	83
List of Procedure Files	84
References	85
Digital-to-Analog Converter Measurements	87
Introduction.	87

Measurement Techniques	88
Notes on the APWIN Procedure Examples	88
Setting Stimulus Levels in dB FS	89
Gain	89
Analog levels expressed in dB FS	89
Gain stability	90
Gain-frequency response	90
Output amplitude for full scale input	99
Maximum Output Amplitude	99
Maximum Signal Level versus Sine Frequency	101
Digital Filter Overshoot and Headroom	103
Noise	108
High-level non-linear behavior	121
Low-level non-linear behavior	130
Jitter Modulation	132
Jitter Tolerance	138
Sampling Frequency Tolerance	139
AES3 / IEC60958 Digital Interface Metadata	140
DITHER ANNEX	147
Dither probability density	148
RPDF Dither	149
TPDF Dither	149
Dithering a low-level tone	150
List of Procedure Files	152
References	153
The Digital Interface	155
Introduction	155
Basic Interface Format	156
Bi-phase coding	156
Unit interval	157
Framing	157
Preambles	158
Audio data	159
Validity bit	160
User bit	160
Channel status bit	161
Parity bit	162
Electrical properties	163
Synchronization	167
Output Port Measurements	168
Output port impedance	168

Output port amplitude	171
Output port balance.	172
Transition times	175
Intrinsic Jitter	176
Jitter transfer function	179
Input Port Characterization	181
Input port impedance.	182
Maximum input amplitude	184
Minimum input signal amplitude and the eye diagram	184
Common-mode rejection	186
Receiver jitter tolerance	187
Signal Characterization	190
Signal Amplitude.	190
Signal Interface jitter	190
Signal symmetry and DC offset.	190
Signal reflections	191
Determining Data handling characteristics	195
Audio data	196
Data transparency	196
Channel Status	196
Validity bit	200
User data	201
Channel Status Annex.	201
Consumer format channel status	201
Professional format channel status	203
List of Files	205
References	205
