THE DIAGNOSIS AND SOLUTION OF JITTER-RELATED PROBLEMS IN DIGITAL AUDIO SYSTEMS

Julian Dunn* and Ian Dennis,
Prism Sound Limited
*Email: JDunn@iee.org

ABSTRACT

Timing jitter can cause the failure of a digital audio interface, or subtle degradation in the quality of an A-D or D-A conversion. This paper presents measurement techniques which can be used in the diagnosis and analysis of jitter-related problems, and gives examples of their application.

1. INTRODUCTION

It is well known that severe timing jitter in AES3 digital audio interfaces [1] can cause loss of lock or loss of data, and recently it has become understood that even small amounts of this interface jitter can affect the sound quality of analogue-to-digital converters (ADCs) and digital-to-analogue converters (DACs). The diagnosis and solution of these problems is still widely misunderstood amongst equipment designers, with the result that system operators are often plagued by jitter problems. Amongst installed systems, instances of interface failure must obviously be 'repaired' or worked around, usually by changing cable types or synchronization schemes;

As part of the development of a more analytical approach to these problems an ad-hock task group within the AES working group on Digital Input/Output Interfacing has defined some parameters and recommended performance limits [2]. The parameters are `intrinsic jitter', `jitter tolerance', and `jitter transfer function'; this paper describes methods for their measurement. Since some of the measurement techniques require the generation of a known jitter signal, the paper describes the design and operation of a simple jitter modulator.

It has been shown that cable losses within the AES3 digital audio interface interact with the modulated data to introduce timing jitter in the transitions of the modulated part of the signal [3,4]. This mechanism has been shown to form a significant contribution to overall jitter in systems with cable runs of more than a few metres. Receiving equipment may be able to reject this `data jitter' by using the more stable transitions to recover a clock - but often it will not. Test signals have been developed to measure susceptibility of equipment to data jitter. These signals are described and some results are shown.

While interface jitter should be tolerated up to a relatively high level before data integrity is threatened, jitter of these levels at the point of sampling in ADCs and DACs (sampling jitter) will produce objectionable audible effects. There is a relationship between interface jitter and sampling jitter because sampling clocks are often derived from an interface signal. This is the normal mode of operation for most equipment, since each installation generally has only one master sync generator. The AES3 receiving circuit normally contains a phase-locked loop (PLL) whose job is to track the incoming transitions and extract the data. Unfortunately, much professional audio equipment which synchronizes ADCs and DACs to an AES3 reference input uses the receiver PLL to drive the sampling clocks directly, rather than employing a second PLL to reject jitter down to low frequencies. Interface jitter is therefore transferred to the converter device either directly or with minimal attenuation. Measurement techniques have been developed that reveal the sensitivity of converters to interface jitter. Results from these measurements reveal a wide disparity between the best and worst devices in this respect.

2. INTERFACE JITTER

Interface jitter is the timing deviation of the transitions in the AES3 data stream from that which may be regarded as 'ideal' i.e. a signal whose transitions occur exactly at quantum intervals as described in the interface specification. The sum of the timing errors of the earliest and latest transitions with respect to this ideal is the peak-to-peak interface jitter. The present interface specification allows 40ns P-P jitter [1, section 6.2.5].

In real systems, interface jitter may be further analyzed in terms of that generated by the sourcing equipment (output jitter or 'FS' jitter) and that which is observed by the receiver as a consequence of the interconnecting cable, which is data-pattern related and is referred to here as data jitter.

2.1 Intrinsic Jitter Measurement

The intrinsic jitter of a piece of equipment is its output jitter when synchronized internally or to a jitter-free source. In the latter case, the intrinsic jitter reflects the quality of the equipment's clock recovery circuit, as discussed in [5]. In the former case this may not be true and measurements may be better.

Figure 1 shows a method for measuring interface jitter using the Prism DSA-1 hand-held interface analyzer. The DSA-1 uses a jitter attenuator to produce a weighting function similar to that described in [2]. It incorporates a stable PLL with low intrinsic phase noise to reject jitter from the incoming signal [6]. The jitter attenuator produces a stabilized timebase which is used to measure the range of deviations of the incoming interface transitions, and thus a peak-to-peak jitter value is derived and displayed. For an intrinsic jitter measurement it is important to eliminate data-jitter effects. For that reason the transitions measured and those applied to the jitter attenuator are those late in the Y-preamble (see section 6.2 of [2]).

2.2 A Jitter Modulator

Many of the measurement techniques described below require a source of sinusoidal jitter controllable in amplitude and frequency. A device to generate this jitter has not hitherto been widely available.

It is possible to generate jitter on a clock by modulating the oscillator control voltage in a PLL that is locked to that clock. This is the technique described in [4] and [7]. This jittered clock can then be used to generate a digital audio interface signal. The jitter is related to the phase modulation, rather than the frequency modulation, of the clock so that the control voltage required to produce a fixed amount of jitter will rise linearly with jitter frequency. This type of jitter modulator is therefore limited in the amplitude of high frequency jitter that can be generated. At frequencies below the PLL corner frequency the control voltage to jitter transfer function depends on the loop filter characteristics. Care must be taken to ensure that the PLL does not add significant levels of noise itself.

The technique used here applies variable delay to a digital audio signal. The jitter is directly related to the variation in delay. This technique has been reported in [8] and [3] for the analysis of jitter transfer function and sampling jitter modulation effects. The jitter modulator used for [3] has now been developed into a commercial product (figure 2) to allow the measurement of jitter tolerance, jitter transfer function, and (interface jitter to) sampling jitter transfer function.

2.3 Jitter Tolerance Measurement

An AES3 digital audio receiver can cope with a jitter up to a threshold amplitude - the jitter tolerance of the device. Above this level the unit fails to decode the signal correctly - normally either occasionally muting or losing `lock' altogether. Jitter tolerance is flat for jitter above the corner frequency of the receiver PLL. At lower jitter frequencies the receiver PLL can track the jitter so tolerance rises. A simple characterisation of receiver tolerance would be to measure the tolerance

level with the stimulating frequency in the flat region and the frequency at which this tolerance has increased by a significant amount - for example 6dB.

The jitter modulator described above has been used to confirm the jitter tolerance of a variety of equipment. The worst tolerance measured so far is a DAC for professional applications. This unit loses lock with more than 25ns (peak-peak) of pseudo-random jitter, equivalent to 0.15 unit intervals (UI, defined as 1/128 of the sample period). Unfortunately it was not possible to perform a full sinusoidal sweep to analyze this behaviour. Most available equipment does have a jitter tolerance that exceeds the minimum 0.25UI recommended in [2].

2.4 Jitter Transfer Function Measurement

The jitter modulator has also been used to measure jitter transfer function. The technique is illustrated in figure 3 - taken from [2]. The modulator takes a low jitter, free-running digital audio source as an input, and the sync output is used to lock an oscilloscope. The device under test (DUT) is set to synchronize with the output of the modulator. The timing of the output signal from the DUT can be directly compared with the reference sync. The jitter gain through the DUT can be measured with sinusoidal jitter of moderate amplitude. The following table shows some results of such measurements:

Jitter frequency kHz	Applied jitter ns pk-pk	Measured jitter ns pk-pk	less no-jitter result	Jitter Gain dB
No input	0	2.5		--
1.0	20	23	20.5	0.2
2.0	20	24	21.5	0.6
4.2	20	14	11.5	-4.8
7.5	20	10	7.5	-8.5
15.0	20	5	2.5	-18.0

These results show a corner frequency at approximately 3kHz and a small amount of jitter peaking around that point. For a complete evaluation of the unit it would be important to take more measurements at frequencies close to the corner frequency to confirm that this unit has a peak gain of less then the 1dB recommended by [2].

Note that this concept of a linear jitter transfer function is a simplification for convenience. Phase detector dead spots can result in a level of intrinsic jitter that is actually reduced as jitter is applied to the source. This occurs because the applied jitter stimulates the phase detector into a linear region of operation so restoring the correct amount of feedback and hence allowing the loop to attenuate the VCO phase noise.

The choice of stimulus jitter level of 20ns (0.12 UI) was made to maintain a good applied-jitter-to-intrinsic-jitter ratio while maintaining the test within the range of normal interface jitter levels.

2.5 Data Jitter

Data jitter is a mechanism by which high-frequency transmission losses cause data-related jittering of the interface transitions, as has been described in [5], [4] and [3]. These losses can occur in cables and in driving and receiving circuits.

The measurement method shown in figure [1] and discussed above is applicable to the measurement of data jitter as well as intrinsic jitter. To measure data jitter, the DSA-1 assesses the timing-variation of transitions in the audio data fields rather than those in the Y-preamble.

Data jitter and any resultant failures are, by their very nature, signal dependent. Therefore there is a requirement to make any measurements of the data jitter in a repeatable manner. A key symptom of the high frequency losses is the reduction in length of recovered short-duration pulses, particularly those in the preambles; the degree of shortening is a signal independent indicator of the loss which result in data-jitter. This `runt-reduction' technique is exploited in the DSA-1 [6].

2.6 Data Jitter Test Signal (J-test Signal)

A test signal has been developed in order to stimulate worst-case levels of data-jitter. This signal has two components. The first is an un-dithered square wave with a period of 4 samples. A cycle of this is shown here in hexadecimal notation (hex):

```
C00000 C00000 400000 400000
```

On conversion to analogue at a sample rate of 48kHz this signal would produce a sine wave with an amplitude of -3.01dBFS at 12kHz.

This is added to an undithered 24 bit square wave of amplitude 1 least significant bit (1 LSB) and dc offset of -1/2 an LSB. This square wave is repeated at low frequency. In the case of the signal used in these tests a rate of 250Hz was selected. This adds an undithered square wave of amplitude -144dBFS and a negative dc offset of -150dBFS. The two values used for this square wave are 0 and -1 (FFFFFF).

The combination of these signals results in the following 192 sample cycle of 24-bit data values:

```
C00000 C00000 400000 400000 (x 24) BFFFFF BFFFFF 3FFFFF 3FFFFF (x 24)
```

The low frequency coherent alternation in the values of the 22 LSBs produces strong jitter spectral components at the repetition rate and its odd harmonics. A low frequency was used to stimulate jitter at a frequency that will not be attenuated significantly by a receiver clock recovery circuit. The high frequency component was selected for convenience when making jitter measurements of DACs; this is discussed in a later section.

The effect of the four data values carried by an AES3 interface modulating a long cable are simulated in figure 4. This shows the lower ones density of the top two data patterns (C00000, 400000) compared with the bottom two patterns (BFFFFF 3FFFFF). The time axis is marked in UI. The left-most transition is the start of the X preamble and only subframe 1 is shown.

As a result of high frequency losses, and the biphase-mark coding scheme, zero-valued data bits (represented by 2UI pulses) produce larger amplitudes than the one-valued bits (two 1UI pulses). The transition following larger amplitude pulses has an increased delay. Hence data jitter correlates with the ones density of the data. This effect is illustrated in figures 5 and 6 of [2].

The effect of data jitter on following equipment depends on their circuit design. Some clock recovery circuits use data transitions throughout the sample frame to derive a timing reference so coupling data jitter to the output. Alternatively, it is possible to design digital interface receivers that are not sensitive to this form of jitter. These receivers only use the static, and therefore more stable, pattern of the preamble to provide a timing reference for the clock recovery circuit. This method is described in section 6.2 of [2].

The J-test signal can be used, in conjunction with a cable, to assess data jitter rejection. The low modulation frequency of J-test was selected to reduce the masking effect of simple jitter attenuation

in the DUT. The output jitter when modulated with J-test is compared with that when the modulation is removed (digital `black'). Any significant difference indicates susceptibility to data jitter.

3. CONVERTER CLOCK JITTER

In considering an A-D or D-A converter, it is easy to overlook the extra 'analogue' input which each has: that which controls the timing of sample conversions. Instinctively one is not surprised that modulation of the sampling clock in the time domain results in distortion of the converted signal which worsens as its frequency is increased.

In the simplified case of a sinusoidal jitter modulation, the distortion takes the form of side-bands whose amplitude is proportional to the degree of jitter and whose separation in frequency from the stimulus is equal to the frequency of the jitter.

In sigma-delta devices, with high levels of out-of-band noise, the effect of sampling jitter might be to raise the converter's noise floor significantly by folding the noise in band. Some oversampling devices have circuitry to reduce or eliminate this effect. Other converter architectures may exhibit different degradation models wherein timing jitter results in modulation of the converted level as well as the phase modulation effect.

Though the effects of sampling jitter at higher frequencies are very audible by their aharmonic nature, spuriae resulting from low-frequency jitter are effectively 'masked' by their proximity to the stimulus; therefore the criteria for sampling jitter in the low-frequency range are realistically rather less stringent [9].

It may be possible to make direct measurements of sample clock jitter in a piece of equipment by examining the clock signals at the converter. However, this is not always convenient, and requires a knowledge of the circuit. It also needs dedicated test equipment to demodulate the clock jitter to a useful spectrum. It is therefore often preferable to infer the sampling jitter by examination of the spectrum of the converted signal assuming that an accurate model for sampling jitter in the converter is known.

3.1 Sampling Jitter Models

The effect of sampling jitter has been modelled in previous papers [7], [9], [8] and [4]. The analysis in [7] and [3] models the effect of sampling at the wrong time (without examining other distortion mechanisms within converters that cause modulation of level with sampling frequency). These models assume that the jitter amplitude is small compared with the period of the audio signal being converted. For an input signal of amplitude A and frequency w_i being sampled with jitter of peak-peak amplitude J and frequency w_j the output signal is:

$$v(t) = A[\cos(wit) - \tfrac{1}{4}Jwi\cos((wi - wj)t) + \tfrac{1}{4}Jwi\cos((wi + wj)t)]$$

This is equivalent to the input signal with sidebands at a spacing equivalent to the jitter frequency.

The level of the jitter sideband relative to the signal is proportional to input frequency and is given by:

$$R_j = 20\log(Jw_i/4) \text{ dB} \qquad \text{(Model 1)}$$

A further form of timing-related distortion can be introduced by converters which have a gain proportional to sampling frequency. The Philips `Bitstream' range of converters has this character [10]. This produces an amplitude modulation effect given by the following equation:

$$v(t) = A[\cos(w_it) + \tfrac{1}{4}Jw_i\cos((w_i - w_j)t) + \tfrac{1}{4}Jw_i\cos((w_i + w_j)t)]$$

Note that the side-bands are at the same frequencies but this time the lower sideband is of the opposite polarity. Summing the two equations produces:

$$v(t) = A[\cos(w_it) + \tfrac{1}{4}J(w_j - w_i)\cos((w_i - w_j)t) + \tfrac{1}{4}J(w_j + w_i)\cos((w_i + w_j)t)]$$

The combination of both effects in this range of converters results in jitter amplitude being proportional to sideband frequency, rather than input frequency. The sideband to signal ratio is given by:

$$R_j = 20\log(Jw_s/4) \text{ dB} \qquad \text{(Model 2)}$$

Where w_s is the sideband frequency, $(w_j - w_i)$ or $(w_j + w_i)$ for the lower and upper sideband respectively.

This effect is not a consequence of delta-sigma or pulse-density modulation (PDM), but a result of the sample frequency gain proportionality. Any DAC with an output that is based on quanta of charge rather than current will produce this relation. Raising the sample rate will produce more quanta of charge per unit time, and hence a higher current for the same data value. This model produces results that agree with [4]; however the model does not agree with the first paragraph of section 4.2 of that paper linking this effect to PDM. Results presented below show some PDM DACs with model 1 behaviour (DACs A, B and D).

Heavily oversampled noise-shaped delta-sigma modulators produce ultrasonic noise at high amplitude. This noise is shown in figure 4 of reference [11]. As this noise signal is concentrated at high frequencies, model 1 indicates that jitter sidebands will have a much higher amplitude than for equivalent signals in the audio band, and so sampling jitter will have a greater impact on the noise floor. This is why the circuit described in reference [11] uses a voltage controlled crystal oscillator (VCXO) based PLL. Another approach is to attenuate the modulator noise after the one-bit DAC but before the sampling point. This technique is used in the converter described in [12].

As the model 2 DAC sideband amplitudes scale with sideband frequency rather than input frequency, so the effect of jitter on the ultrasonic noise from the modulator output is reduced by the same proportion. In a bad case this produces a noise floor that rises with frequency - as shown in figure 16 of [3].

3.2 Spectrum Analysis for Jitter Assessment

The aharmonic nature of jitter-related artifacts means that they are potentially much more audibly objectionable than simple harmonic distortion. It is therefore important to be able to detect and measure jitter-related artifacts at very low levels if sonic quality is to be maximized; this is increasingly relevant given the ever-improving dynamic range of modern data converters. This requirement dictates two particularly important criteria for the spectrum analysis equipment.

Models show that distortion artifacts resultant from sampling jitter are proportional in amplitude to the signal being converted. If we are to measure the jitter-induced components accurately it is therefore important that the FFT analyzer have adequate 'simultaneous' dynamic range - i.e. the numeric precision of the analyzer must be such as to allow adequate representation of small signals in the presence of much larger ones. In this, adoption of a floating point representation is not specifically useful, since the mantissa must retain adequate word-length to cover the simultaneous dynamic range requirement, with enough surplus precision to allow the range to be maintained over the considerable number of operations involved in a large FFT. For state-of-the are data converters, this requirement comfortably exceeds the capability of 24-bit fixed-point or 24+n-bit floating-point architectures.

The dynamic range of the analyzer's window-function is also important. Since the number of audio samples used by the analyzer to construct each FFT is finite, an idealized line-spectrum cannot be calculated; instead, each component is distorted by broadening and by the addition of side-lobes. These two effects can generally be traded off by selection of an appropriate window function. The ratio of the stimulus to the side-lobes can be considered as the dynamic range of the window function. Unfortunately, the appearance of the window-induced side-lobes can often resemble jitter-induced sidebands, or the 'skirt' of a window-function might resemble the effect of low-frequency phase noise. It is therefore important that a wide-dynamic-range window is used in the measurement of jitter artifacts.

The analyzer used for the FFT measurements in this paper employs a 48+n-bit floating point architecture, and has over 143dB dynamic range available from its widest window function.

3.3 Example Digital to Analogue Converter Measurements

Six DACs (DACs A to F inclusive) were measured in the preparation of this paper. Owing to space constraints, many of the results have to be summarised.

3.3.1 Jitter Attenuation

Figure 5a shows the output spectrum of DAC B when driven by a 12kHz tone at 0dB (0, +FS, 0, -FS) with jitter at 500Hz and 5ns pk-pk. The equation for model 1 predicts sampling jitter sidebands of -80.51dB at 11.5 and 12.5kHz for no jitter attenuation.

This spectrogram shows a noise floor that has `skirts' within 1kHz of the modulating tone, and discrete sidebands. The main sidebands are at the sum and difference frequencies. The next two sidebands are at twice these frequencies. These reflect 2nd harmonic distortion of the jitter signal and are at separations of 1010Hz from the main lobe. There are also sidebands at +/- 1150Hz, which remained in the absence of the jitter.

The ratio between individual sideband amplitude and main lobe was measured to be -80.9dB at 11.5kHz and 81.2dB at 12.5kHz for lower and upper sidebands respectively. This indicates that there is no jitter attenuation at 500Hz.

Figure 5b is the spectrum with the jitter frequency raised to 4.9kHz. All other conditions remaining the same. The main jitter sidebands have separated and reduced in level to -94.7dB at 7.1kHz and -95.1dB at 16.9kHz. This indicates jitter attenuation of 5dB at 5kHz, suggesting a PLL corner frequency of 2-3kHz. A description of this unit, [11], specifies that the PLL corner frequency is 2.38kHz.

The other DACs measured showed the following results:

DAC	11.5kHz	12.5kHz	500Hz atten	7.1kHz	16.9kHz	5kHz atten
Model 1	80.51	80.51		80.51	80.51	n/a
A	81.4	81.7	none	79.4	80.2	none
B	80.9	81.2	none	94.7	95.1	5dB
C	81.0	81.2	none	81.5	82.4	<2dB
D	80.5	80.6	none	105.7	106.0	25dB
Model 2	80.90	80.17	n/a	85.10	77.53	n/a
E1	79.9	79.4	none	108.5	101.6	24dB
E2	101.3	100.8	20dB	122	119	>35dB
F	78.8	78.1	none	84.0	76.4	none

The sideband amplitudes are in dB with respect to the stimulus. The results calculated from the models are also shown in the table. For the units without jitter attenuation these show a good match with the measurements.

Note that the results show that the PLL corner frequencies of these samples vary from <50Hz for E2 to DACs A and F, which have no indication of jitter attenuation below 5kHz. DAC E has two modes of operation, E1 has a PLL corner frequency of approximately 1.2kHz (figure 6a) while E2 has a corner frequency of about 30Hz (figure 6b). In the latter mode the low frequency intrinsic jitter is significant. This produces skirts to the main component in the figure, illustrating the design trade-off between intrinsic jitter and jitter attenuation.

3.3.2 Data jitter susceptibility

Surprisingly, the effects of Data Jitter are normally worse for low-level audio signals, since the twos-complement coding means that for a very small signal, nearly all the data bits change in unison. If the effects of data jitter reach an A-D or D-A converter unfiltered (and if the frequency of the jitter-inducing signal is low as well as its level, this is almost inevitable) a distortion results, as well as the possibility of a strange crosstalk effect between A and B channels, or from a digital audio reference signal to an audio output.

Figure 7 shows the effect of the jitter test signal is revealing jitter behaviour. It was connected to the inputs of the respective DAC through a 100m length of screened audio cable (150pF/m, 90mW/m). This cable is used to provide the bandwidth restriction required to induce data-jitter. The jitter in the data edges at the DAC input interface was measured to be approximately 12ns. This amount of jitter should produce -72.9dB sidebands for model 1 or -73.1 and -72.7dB sidebands for model 2.

DAC A and DAC B both show sensitivity to data jitter. DAC A shows no attenuation below 20kHz as the level of the sidebands are commensurate with those of the applied square wave up to that point. DAC B shows the effect of the 2.38kHz PLL corner frequency as the higher harmonics in the jitter signal are attenuated. DAC E, which is operating in E1 or 1.2kHz bandwidth mode, shows the sidebands at about -106dB. This indicates attenuation of >32dB. This device is therefore insensitive to data jitter.

4. CONCLUSION

Several tools have been developed to measure the digital audio interface parameters discussed in [2], including a jitter modulator to produce known and controllable amounts of jitter so that measurements of jitter transfer function and jitter tolerance can be made.

Mathematical models to relate sampling jitter levels and resultant distortion products have been refined and measurements have been made using a wide dynamic range spectrum analysis tool. Results indicate a good correspondence. The jitter attenuation recorded by results from some of the converters indicate that, as well as being impractical, it is not necessary to specify maximum interface jitter levels commensurate with sampling jitter levels necessary to ensure good DAC performance; as long as converter designers provide adequate jitter attenuation.

A test signal has been devised to allow consistent assessment of data jitter susceptibility of clock recovery systems. Measurements made with this signal has shown the susceptibility of some DACs to converting data jitter to sampling jitter, but this is not universally the case. The response of one of the DACs demonstrated that it is possible to make clock recovery systems that do not have this behaviour. Therefore sampling jitter resulting from data jitter is simply the result of poor equipment design and not, as has been suggested (among others by [4]), a fundamental shortcoming of the interface specification.

5. ACKNOWLEDGMENTS

The authors would like to thank the technical staff of Metropolis Mastering, London, for the opportunity to evaluate a variety of digital audio equipment; also for their advice based on operational experience in banishing jitter-related problems, which has been invaluable. Thanks are also due to Barry McKibben and Michael Gerzon with assistance with the mathematical model used to simulate the cable for figure 4.

6. REFERENCES

[1] AES3-1992 - ` Recommended Practice for Digital Audio Engineering - Serial Transmission Format for Two-Channel Linearly Represented Digital Audio Data' J. Audio Eng. Soc., vol 40 No. 3, pp 147-165 (June 1992)

[2] Dunn J., McKibben B., Taylor R. & Travis C. - 'Towards Common Specifications for Digital Audio Interface Jitter' Preprint 3705, presented at the 95th AES Convention, New York, October 1993

[3] Dunn, Julian. - `Jitter: Specification and Assessment in Digital Audio Equipment'. Preprint 3361, presented at the 93rd AES Convention, San Francisco, October 1992.

[4] Dunn, Chris and Hawksford, Malcolm Omar. - `Is the EBU/SPDIF Digital Audio Interface Flawed ?'. Preprint 3360, presented at the 93rd AES Convention, San Francisco, October 1992.

[5] Dennis, Ian - `Jitter in Digital Audio Systems - Effects of Equipment Interconnection and Design', first presented at Digitale Studio Konzeptz seminar, Swiss Section Audio Eng. Soc. 13th September 1993.

[6] Blair, I., Dennis, I., Dunn, J., & Spencer, E. - `New Techniques in Analyzing the Digital Audio Interface'. Preprint 3230, presented at the 92nd AES Convention, Vienna, March 1992

[7] Harris, Steven - 'The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta-Sigma ADCs' *J. Audio Eng. Soc.*, vol 38 No. 7/8, pp 537-542 (July/August 1990)

[8] Fourre R. D. - 'Jitter, Jitter, Jitter ...' Application note AP-03, published by UltraAnalog Inc, Fremont, California, September 1992.

[9] Dunn, Julian. - `Considerations for Interfacing Digital Audio Equipment to the Standards AES3, AES5, AES11'. Published in `Images of Audio', the *Proceedings of the 10th International Conference*, London, September 1991. pp 115-126.

[10]Data sheet for TDA1547 Dual top-performance bitstream DAC, preliminary specification, Philips Semiconductors, September 1991.

[11]Green S.R., Harris S. & Wilson B. - 'An 18-bit Delta-Sigma D/A Processor System Achieving Full-Scale THD+N>100dB' Preprint 3416, presented at the 93rd AES Convention, San Francisco, October 1992

[12]Sooch N.S., Scott J.W., Tanaka T., Sugimoto T., and Kubomura C. - `18 bit Stereo D/A Convertor with Integrated Digital and Analogue Filters' Preprint 3113, presented at the 91st AES Convention, October 1991.

FIGURES

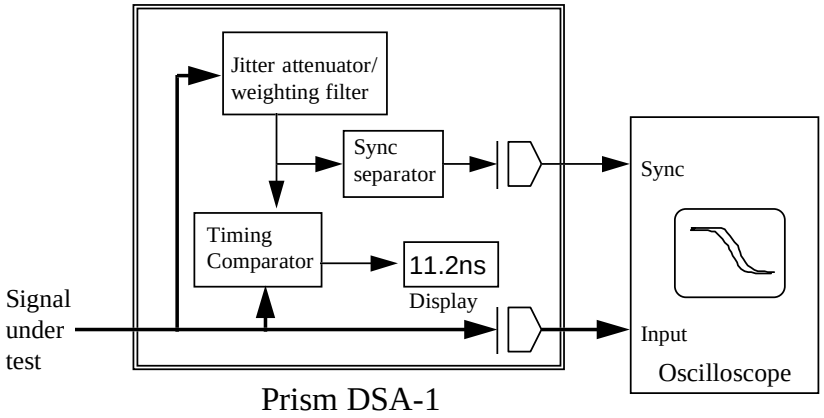


Figure 1 - Weighted interface jitter measurement

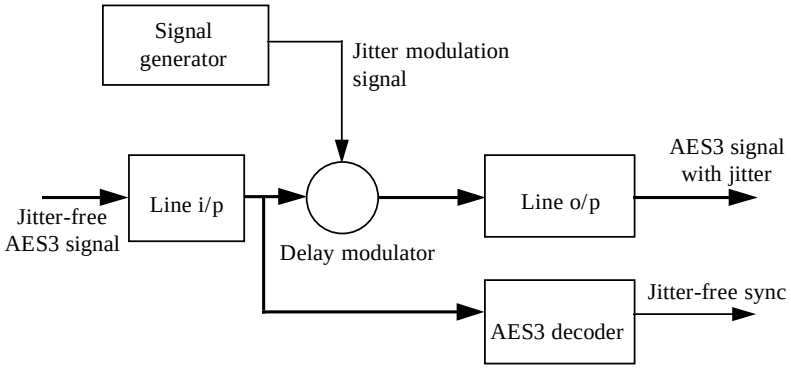


Figure 2 - Jitter modulator block diagram

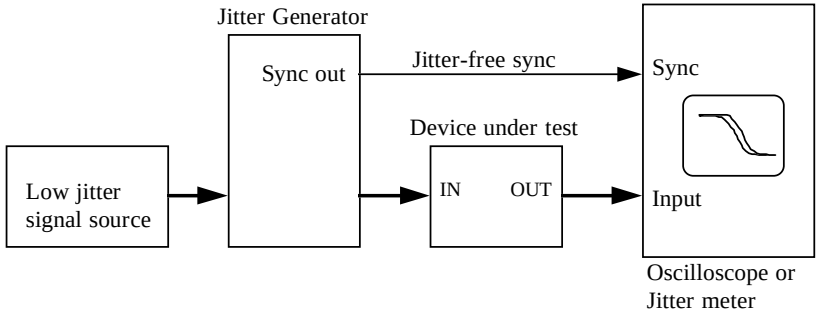
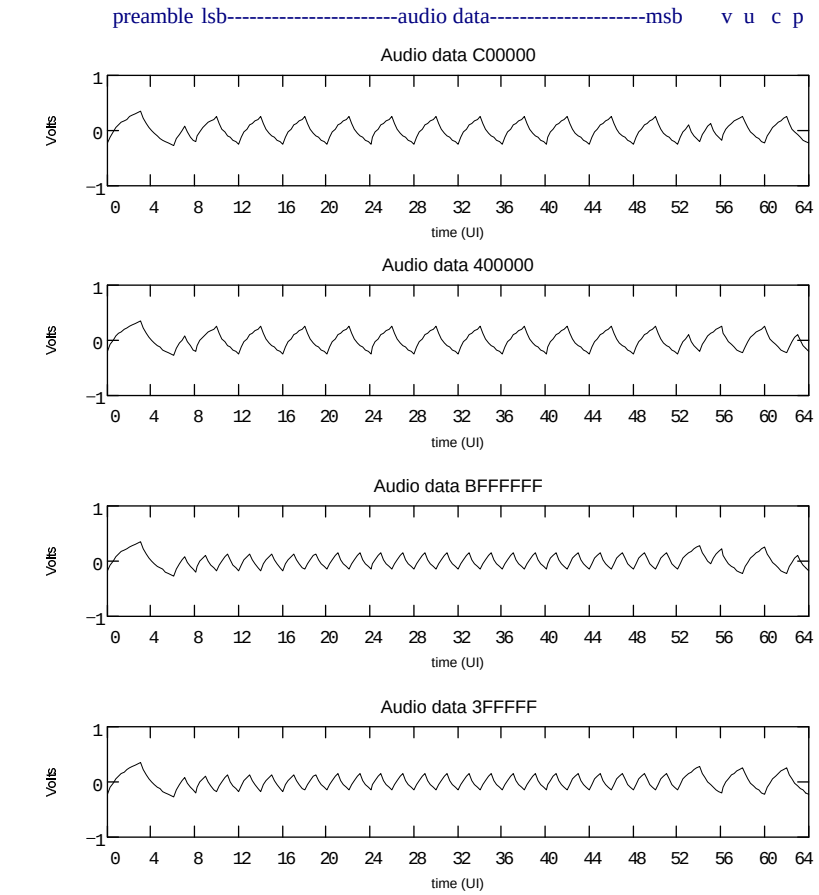


Figure 3 Jitter tolerance and transfer function measurement



Simulated output after transmission through a 100m length of cable with capacitance 150pF/m and resistance 90ohms/km

Figure 4 A test signal for data jitter (J-test)

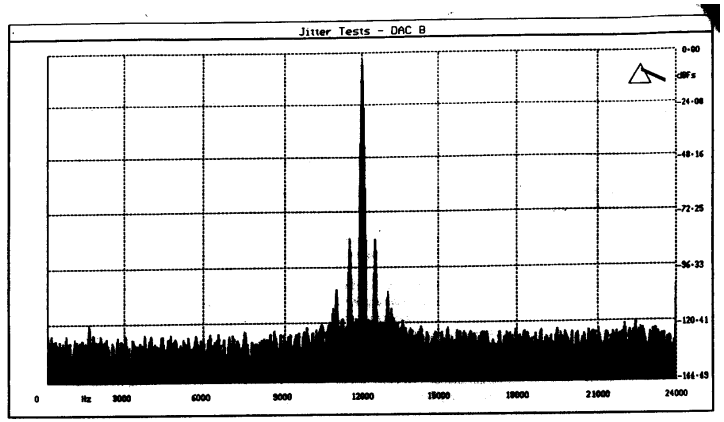


fig 5a

fig 5b

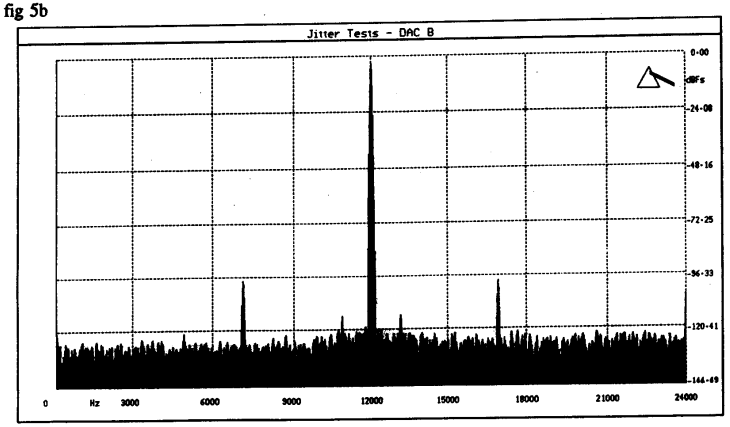


Figure 5 FFT plots showing jitter attenuation characteristics in a DAC

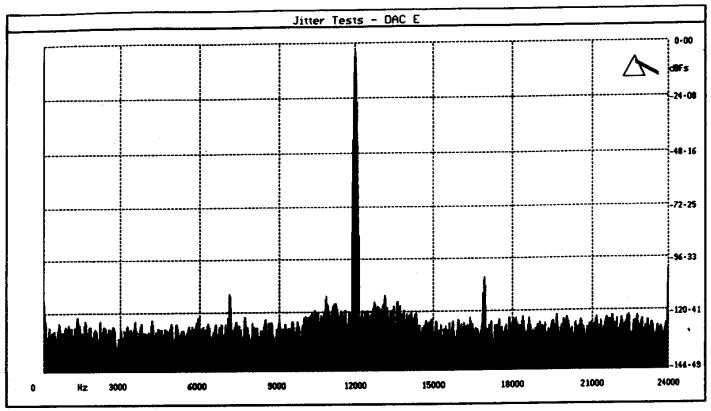


fig 6a

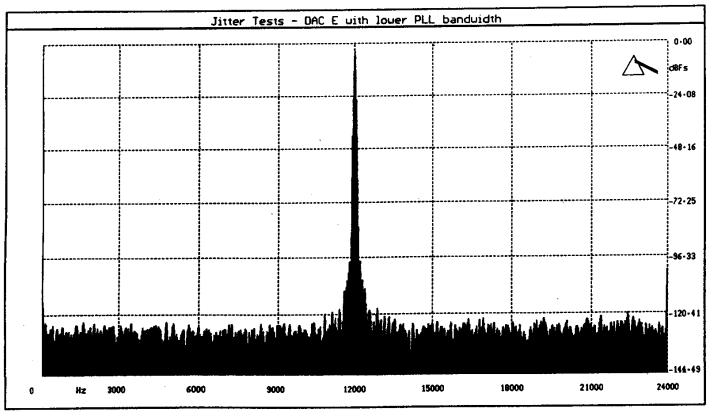


fig 6b

Figure 6
FFT plots showing the trade-off between PLL bandwidth and low-frequency intrinsic jitter

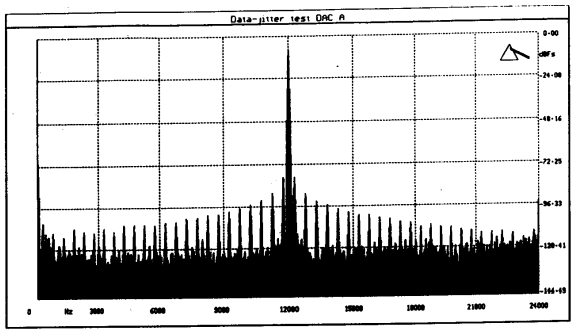


fig 7a

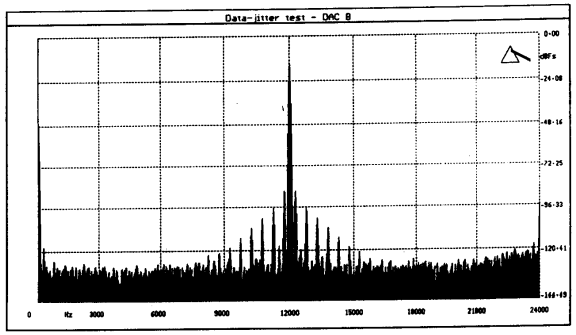


fig 7b

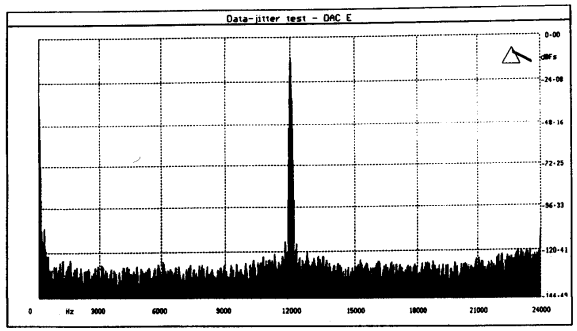


fig 7c

Figure 7 - The responses of three converters to the J-test signal

Figure 7 The responses of three converters to the J-test signal